WHAT IS CLAIMED IS:

1. A method for correcting back-gating in a power FET caused by drain voltage changing rapidly from a higher voltage level to a lower voltage level comprising:

providing an input signal to a sensing FET located on a common substrate as said power FET, wherein said input signal is also provided to said power FET;

forming an output signal from said sensing FET, wherein said output signal is substantially proportional to a shift in threshold voltage of said sensing FET caused by effects of back-gating;

modifying said input signal using said output signal via a feedback path; and

providing said input signal to said power FET, wherein said input signal controls said power FET such that a shift in threshold voltage of said power FET caused by effects of back-gating are substantially reduced.

2. The method of claim 1, wherein the step of forming an output signal from said sensing FET further comprises a step for generating a voltage across a resistor connected to a source of said sensing FET, wherein said voltage across said resistor measures current flowing from said source of said sensing FET.

3. The method of claim 1, wherein the step of modifying said input signal using said output signal via a feedback path further comprises the steps of:

forming an error signal using said output signal;

amplifying said error signal to form an amplified error signal; and

adjusting or generating said input signal using said amplified error signal.

4. A method for correcting back-gating in a power FET caused by drain voltage changing rapidly from a higher voltage level to a lower voltage level comprising:

sensing said back-gating as a measure of current flowing through a sensing FET, wherein said sensing FET is located on a common substrate as said power FET, wherein a gate voltage is connected with a gate of said sensing FET and a gate of said power FET;

generating a compensation signal using a voltage associated with said measure of current flowing through said sensing FET; and

adjusting or generating said gate voltage via a feedback path using said compensation signal such that said adjusted or generated gate voltage compensates against effects of back-gating.

5. The method of claim 4, wherein said voltage associated with said measure of current flowing through said sensing FET is a voltage across a resistor connected with said sensing FET.

6. The method of claim 4, further comprising a step of amplifying said compensation signal before the step of adjusting or generating said gate voltage using said compensation signal.

7. The method of claim 6, where the step of amplifying said compensation signal is performed using a modified current mirror voltage reference source circuit.

8. The method of claim 4, further comprising a step of inverting said compensation signal before the step of adjusting or generating said gate voltage using said compensation signal.

9. The method of claim 8, where the step of inverting said compensation signal is performed using a modified current mirror voltage reference source circuit.

10. An apparatus for correcting back-gating in a power FET caused by drain voltage changing rapidly from a higher voltage level to a lower voltage level comprising:

a sensing FET sensing said back-gating as a measure of current flowing through said sensing FET, wherein said sensing FET is located on a common substrate as said power FET, wherein a gate voltage is connected with a gate of said sensing FET and a gate of said power FET;

a circuit generating a compensation signal by using a voltage associated with said measure of current flowing through said sensing FET; and

a feedback path using said compensation signal to adjust or generate said gate voltage such that said adjusted or generated gate voltage compensates against effects of back-gating.

11. The apparatus of claim 10, wherein said voltage associated with said measure of current flowing through said sensing FET is a voltage across a resistor connected with said sensing FET.

12. The apparatus of claim 10, further comprising an amplifier circuit for amplifying said compensation signal before using said compensation signal for adjusting or generating said gate voltage.

13. The apparatus of claim 12, wherein said amplifier circuit comprises a modified current mirror voltage reference source circuit.

14. The apparatus of claim 10, further comprising an inverting circuit for inverting said compensation signal before using said compensation signal for adjusting or generating said gate voltage.

15. The apparatus of claim 14, wherein said inverting circuit comprises a modified current mirror voltage reference source circuit.

16. A system for correcting back-gating in a power FET caused by drain voltage changing rapidly from a higher voltage level to a lower voltage level comprising:

means for sensing said back-gating as a measure of current flowing through a sensing FET, wherein said sensing FET is located on a common substrate as said power FET, wherein a gate voltage is connected with a gate of said sensing FET and a gate of said power FET;

means for generating a compensation signal using a voltage associated with said measure of current flowing through said sensing FET; and

means for adjusting or generating said gate voltage via a feedback path using said compensation signal such that said adjusted or generated gate voltage compensates against effects of back-gating.

17. The system of claim 16, wherein said voltage associated with said measure of current flowing through said sensing FET is a voltage across a resistor connected with said sensing FET.

18. The system of claim 16, further comprising means for amplifying said compensation signal before the step of adjusting or generating said gate voltage using said compensation signal.

19. The system of claim 18, where the means for amplifying said compensation signal further comprises a modified current mirror voltage reference source circuit.

20. The system of claim 16, further comprising means for inverting said compensation signal before the step of adjusting or generating said gate voltage using said compensation signal.

21. The system of claim 20, where the means for inverting said compensation signal further comprises a modified current mirror voltage reference source circuit.